

Yamanotoo Hardware Reference

HISTORY

- 3dec2023: Initial release
- 7dec2023: First public release
- 15feb2024: Clarified OFFR register
- 9oct2924: Added SUBOFF bits in CFGR
- 13oct2024: Repurposed LOW bit as MDIS in CFGR

1. Configuration registers

Configuration Registers reside on top of page 1 (4000-7FFFh)

There are 4 registers from 7FFC to 7FFFh.

After reset or power-up, only ENAR is writable and no register is readable.

To enable access to all registers set bit REGEN (See 2.1 ENAR register)

Address	Register Name	Reset Value	Remarks
7FFFh	ENAR	00h	Features enable
7FFEh	OFFR	00h ¹	Mapper offset
7FFDh	CFGR	00h ²	Configuration and Control
7FFCh	-	<undef>	-

¹ Only at power-on. Cpu reset does not change value

² Default values may be different when Features are enabled by default in a customized core

2. Register details

2.1. ENAR register (7FFFh)

This is the only register you can write when REGEN is 0.

It is NOT readable until REGEN is 1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	-	WREN	-	-	-	REGEN
			RW				RW

- WREN: Write enable. Set to 1 to enable writes to flash rom
- REGEN: Registers enable. Setting this bit allows writing to all other registers and all register readability.

2.2 OFFR register (7FFEh)

This register is only readable and writable when REGEN=1 (See 2.1 ENAR)

OFFR value is added to mapper writes, multiplied by 4, causing an offset in units of 32 Kbyte (4 x 8 KByte) in segment selection for the written bank.

Note that change OFFR register has no effect in any bank until the mapper register is written.

I.e. *when writing* the mapper, internal segment selection takes (OFFR * 4) + write value.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OFFSET value (8 bit wide)							
RW							

2.3 CFGR register (7FFDh)

This register is only readable and writable when REGEN=1 (See 2.1 ENAR)

CFGR value is used to control functions or modes of operation.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
-	-	SUBOFF		K4	ROMDIS	ECHO	MDIS ³
		RW		RW	RW	RW	RW

- SUBOFF. Sub-offset. This provides 2 additional lower bits for offset register, to provide 8 kbyte granularity for offset. See section 2.2
- K4. Changes mapper configuration from Konami5 (SCC) to Konami4 for compatibility with game compilations including non-SCC games.
- ROMDIS. Setting this bit disables access to flash rom. This is automatically set during boot when the DEL key is pressed. **You need to clear this bit in software to be able read/write the flash rom.**
- ECHO. Setting this bit allows the built-in PSG to respond to the port number of the internal PSG of the MSX, causing music intended for the internal PSG to be played too in the Yamanooto and be heard through the stereo output of the cartridge. This is automatically set during boot when you press the HOME key.
- MDIS. This bit disables mapping so you avoid mapper changes with small (up to 32 kbyte) roms that poke the switching area. Usually this is a problem only in K4 mode. **Remember to reset this bit to make changes again.**

Note that CFGR bits are **not reset** during a CPU reset so they remain set until cleared by software or power-off.

³ This bit was (psg) LOW, which caused the built-in psg to sound with lower volume. It had no use so we re-purposed this bit.